Chapter 3: Digital Input Conditioning

Digital Input seems pretty cut and dried. An input voltage at Vdd is recognized as a digital HIGH (binary 1). An input voltage at Vss (ground) is recognized as a digital LOW (binary 0). However, what if the BASIC Stamp input is not connected to either? What state will it assume, if any? What if the input is 2.5 V?

Devices which supply an input to the BASIC Stamp may not always provide +5 V for a HIGH and 0 V for a LOW. It is important to understand the digital input characteristics of the BASIC Stamp. Also important are the proper techniques of conditioning signals from mechanical input devices such as pushbuttons. Conditioning from electronic input devices is also frequently necessary as well.

In this chapter we will explore the input characteristics of the BASIC Stamp, the basic operation of a BJT (Bipolar Junction Transistor) and mechanical and electronic switch interfacing.

ACTIVITY #1: MEASURING THE THRESHOLD VOLTAGE

A HIGH level, or logic 1, is typically the positive voltage of the system. A LOW level, or logic 0, is typically the negative supply, or ground reference, of the system. For the BASIC Stamp these are labeled Vdd (+5 V) and Vss (0 V, which is "ground").

What if the voltage at the input were 3.5 V? Is this HIGH or LOW? What about 2.5 V? 2.0 V? 1.0 V? Since a digital system only can be one of two states, at what input voltage do the HIGH and LOW states transition? This activity will measure the threshold voltage below which the input is LOW and above which the input is HIGH. An Analog to Digital Converter (ADC) will be used to measure and plot the voltage levels at the input. A full discussion of the ADC is covered in Chapter 6.

Parts Required

(1) ADC0831 Analog to Digital Converter
(1) 10 kΩ Single-Turn Potentiometer
(2) 220 Ω Resistor
(1) LED – Red

√   Construct the circuit in Figure 3-1.
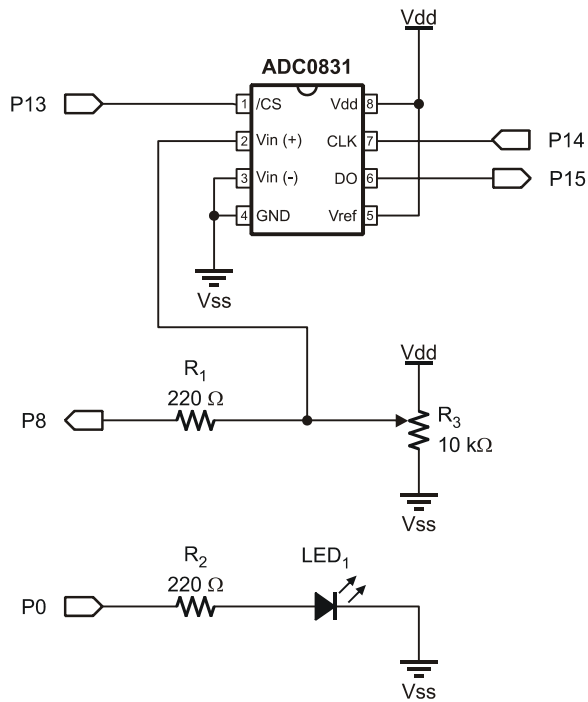
Figure 3-1
Analog and Digital
Data Monitoring
Circuit

Example Program: DataMonitoring.bs2

√   Enter and run the BASIC Stamp program DataMonitoring.bs2.

```
' -----[ Title ]---------------------------------------------------------------
' Process Control - DataMonitoring.bs2
' Monitors and Plots Analog and Digital Data
' {$STAMP BS2}
' {$PBASIC 2.5}

' -----[ Declarations ]-------------------------------------------------------
DigDataIn    VAR Bit      ' Digital input data
ADC_DataIn   VAR Byte     ' Analog to Digital Converter data
```

```
LED          PIN 0         ' LED output pin
DigIn        PIN 8         ' Digital input pin monitored
ADC_CS       PIN 13        ' ADC Chip Select pin
ADC_Clk      PIN 14        ' ADC Clock pin
ADC_Dout     PIN 15        ' ADC Data output

' -----[ Initialize ] -------------------------------------------------
OUTPUT LED                 ' Set LED as output
PAUSE 1000                 ' Allow connection to stabilize

' -----[ Main Routine ]------------------------------------------------
DO
  GOSUB ReadData
  LED = DigIn
  GOSUB PlotData
  PAUSE 500
LOOP

' -----[ Subroutines ]-------------------------------------------------
ReadData:                  ' Read ADC 0831
  LOW ADC_CS               ' Enable chip
  DigDataIn = DigIn        ' Read digital input value to coincide with ADC read
  SHIFTIN ADC_Dout, ADC_Clk, MSBPOST,[ADC_DataIn\9] ' Clock in data from ADC
  HIGH ADC_CS              ' Disable ADC
RETURN

PlotData:                  ' Send data to StampPlot
  DEBUG IBIN DigDataIn,CR ' Plot indicated binary value
  DEBUG "[",              ' Bracket for StampPlot math operation
        DEC ADC_DataIn, ' Analog data
        ",*,.0196]",CR  ' Convert ADC value to voltage by StampPlot
RETURN
```

√   Close the Debug Terminal.
√   Load StampPlot with the macro sic_pc_data_monitoring.spm
√   Connect and plot.
√   Adjust the potentiometer. The analog voltage and plotted value should change
      accordingly.   LED$_1$, on the BASIC Stamp output pin P0, indicates the
      HIGH/LOW status of P8.
√   Note the voltage at which the input P8 changes between HIGH and LOW logic
      levels. This is the threshold voltage.

Figure 3-2 shows an example test in which the threshold voltage was found to be
approximately 1.45 V. The digital trace at the top goes high and low as the analog
voltage goes above or below the threshold voltage.
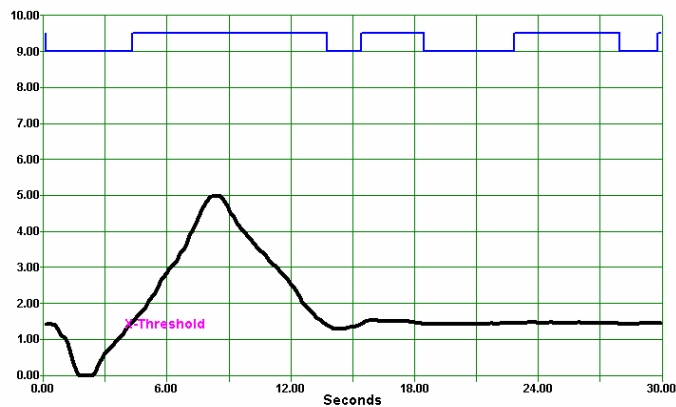
Figure 3-2
Logic Threshold
Voltage Plot

Manufacturer data sheets provide guaranteed threshold voltage for a device. Legal HIGH and LOW values are considered above and below these levels.

- V_{IH} – Voltage In-High: Voltage above which assured to be HIGH on the input.
- V_{IL} – Voltage In-Low: Voltage below which assured to be LOW on the input.

For the BASIC Stamp:

- $V_{IH} = 2.0$ V
- $V_{IL} = 0.8$ V

The BASIC Stamp has a very clear and repeatable threshold. Halfway between V_{IH} and V_{IL} is the 1.4 V TTL logic threshold at which the input will change sensed states. Not all digital devices have the same thresholds. Additionally, some inputs may employ Schmitt Triggers, or hysteresis, where threshold levels differ, depending on whether the voltage is increasing or decreasing to change states. The concept of hysteresis will be explored further in later chapters.

PROGRAM DISCUSSION

LED_1 in Figure 3-1 is used to indicate the state of P8: LED On = HIGH.

The potentiometer may simply be thought of as a variable voltage divider, such as in Figure 3-3. Keep in mind that each of these potentiometer voltages, V(a), V(b), V(c), and V(d), occurs as the knob on the potentiometer is turned to certain positions. Also keep in mind that each of the voltages can be applied to P8 in Figure 3-1.

Figure 3-3 10 kΩ Voltage Divider *(Do Not Build)*
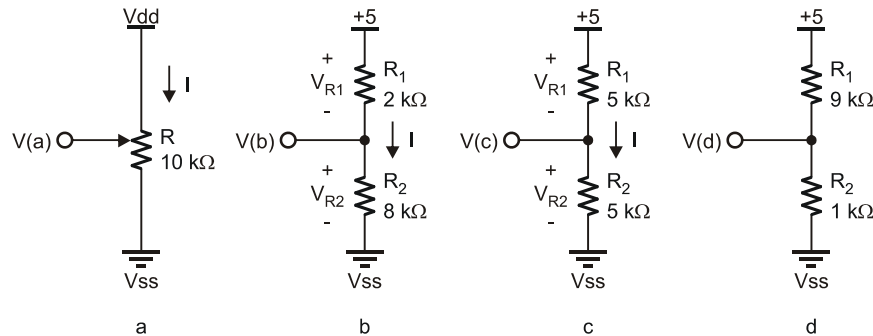
The voltage output is a function of the voltage drop to ground across the lower portion of the potentiometer illustrated by R2 in Figure 3-3. Kirchoff's Voltage Law states that the "algebraic sum of the voltages in a series circuit must equal the supply voltage." The voltage dropped across R1 and R2 must equal the supply voltage, Vdd, of 5 V. Using Ohm's Law, the circuit may be analyzed:

Current = Voltage / Resistance or I = V/R

The total resistance must equal the value of the potentiometer, 10 kΩ.   As such, the current flow through the resistor is:

I = V/R = 5 V/10 kΩ = 0.5 mA

The wiper only changes where it is tapping and splitting the total resistance. The voltage across R_2 for Figure 3-3b can be found by:

$$V_{R2} = I(R_{R2}) = (0.5 \text{ mA})(8 \text{ k}\Omega) = 4 \text{ V}$$

How much voltage is dropped across R_1 in Figure 3-3b?

$$V_{R1} = (IR_{R1} = (0.5 \text{ mA})(2 \text{ k}\Omega)) = 1 \text{ V}$$

The total voltage of the series circuit in Figure 3-3b is:

$$V_{R1} + V_{R2} = 1 \text{ V} + 4 \text{ V} = 5 \text{ V}$$

Kirchoff's Voltage Law is upheld in that the sum of the voltages equals the supply voltage.

The voltage divider formula may also be used to find V_{R2}:

$$V_{R2} = Vdd(R_{R2}/R_1 + R_2)) = 5 \text{ V}(8 \text{ k}\Omega/(8 \text{ k}\Omega + 10 \text{ k}\Omega) = 5 \text{ V}(8 \text{ k}\Omega/10 \text{ k}\Omega) = 4 \text{ V}$$

For Figure 3-3c, what is V_{R2}? Without using any math, we can see the resistances are equal; therefore, the voltage drops must be equal to one-half of the supply voltage.

√   Calculate V_{R2} for Figure 3-3d.

This voltage is measured by the analog to digital converter and used as input to P8. When the voltage divider produces a voltage at or above 1.45 V, P8 senses a HIGH. When below 1.45 V, P8 senses a LOW.

The analog to digital converter is measuring the voltage, 0 to 5 V, and the BASIC Stamp is reading the ADC using the **SHIFTIN** instruction. The voltage is represented by 8-bits for a digital value from 0 to 255. **DEBUG** sends this value to StampPlot in the form of:

```
DEBUG "[ADC_DataIn,*,.0196]"
```

255 **x** .0196 = 4.998 V

The brackets instruct StampPlot to perform math on the data string prior to plotting it. For a digital value of 128, the string would be **[128,*,.0196]**.

StampPlot will perform the math, plot and display 128 * 0.0196 or 2.51, representing the voltage. Deeper discussions on ADCs and scaling data are in later chapters.

Saving digital input is performed within the routine to read the ADC, in an attempt to read both the ADC and digital input at the same time.   The ADC value and the digital value may not track perfectly depending on how quickly the analog level changes.

Challenge 3-1: Reversing the Potentiometer Supply Voltage

√   Note the direction of rotation needed to achieve an increasing voltage.
√   Reverse the Vdd and Vss connections to the potentiometer.

What has changed when rotating the potentiometer? Explain why this change has occurred. (Hint: Refer to Figure 3-3a, and consider what occurs when Vss and Vdd are swapped).

ACTIVITY #2: NIGHT-LIGHT PROCESS

The input of the BASIC Stamp changing between HIGH and LOW at a fixed voltage can provide a simple means of control using analog signals. The input simply needs to go above and below the threshold level for the controller.

In this activity, a photoresistor will be added to the bottom of the variable resistor in the ADC circuit from Activity 1. This modified circuit creates a light-controlled voltage divider input to the BS2 for control of a light (the LED) at a certain level of darkness.

Parts Required

Circuit from Activity #1 (Figure 3-1 on page 46)
(1) Photoresistor

√   Modify the circuit as shown in Figure 3-4 by adding the photoresistor between the potentiometer and Vss. Do not modify the ADC or LED portions of the circuit.
√   Re-run the program DataMonitoring.bs2, if needed.
√   Close the Debug Terminal.
√   Run StampPlot macro sic_pc_data_monitoring.spm.
√   Connect and plot.
√   Allow the photoresistor to be exposed to 'daylight levels' of light.
√   Adjust the potentiometer for a daylight voltage of 1.0 V.

√ Cast a shadow over the the photoresistor. What happens to voltage? When does your light energize?
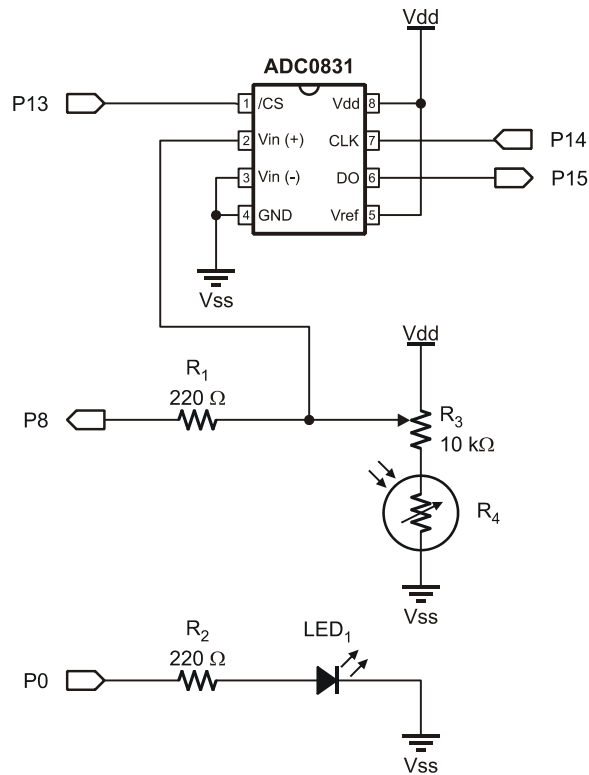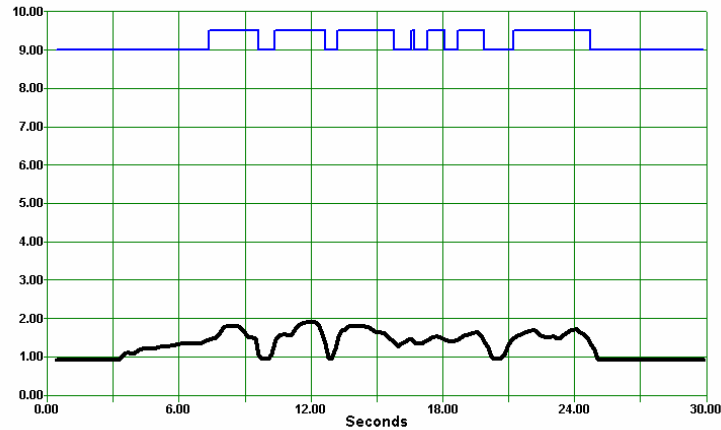

Figure 3-4
Photoresistor Added
to Potentiometer
Portion of the Circuit

In the CdS (Cadmium Sulfide) photoresistor, light photons excite electrons and allow them to flow more freely. This in turn changes the resistance. As light level increases, resistance decreases. In our case, as we shade the photoresistor, its resistance increases.

A greater voltage is dropped on the bottom half of the voltage divider (from the wiper to Vss). When the voltage drop to ground increases above the threshold voltage, the BASIC Stamp senses P8 as a logical HIGH.

Figure 3-5
Night-Light
Plot

Challenge 3-2: Photographic Darkroom Alarm

√   Modify the circuit to exceed the threshold when excess light falls on the sensor. Draw your circuit modifications. Discuss settings and results.

ACTIVITY #3: UNCOMMITED INPUTS AND CONDITIONING SWITCHES

An uncommitted input is one not dedicated to a voltage potential, is said to be "floating" and may not be sensed by the BASIC Stamp as a definite logic HIGH or LOW. Simply connecting a mechanical switch between the input and Vdd leaves the input floating when the switch is open. Current flow to Vdd or Vss is necessary to "commit" the input (when in the open condition). This exercise will help make this concept clear.

Parts Required

(1) ADC0831
(2) Resistors – 220 Ω
(1) Resistor – 1 kΩ
(1) Resistor – 10 kΩ
(1) Pushbutton – Normally Open
(1) LED – Red

√   Replace the photoresistor circuit Figure 3-4 with the pushbutton circuit as shown in Figure 3-6.
√   Re-run the program DataMonitoring.bs2
√   Close the Debug Terminal.
√   Run the StampPlot macro sic_pc_data_monitoring.spm.
√   Connect and plot.
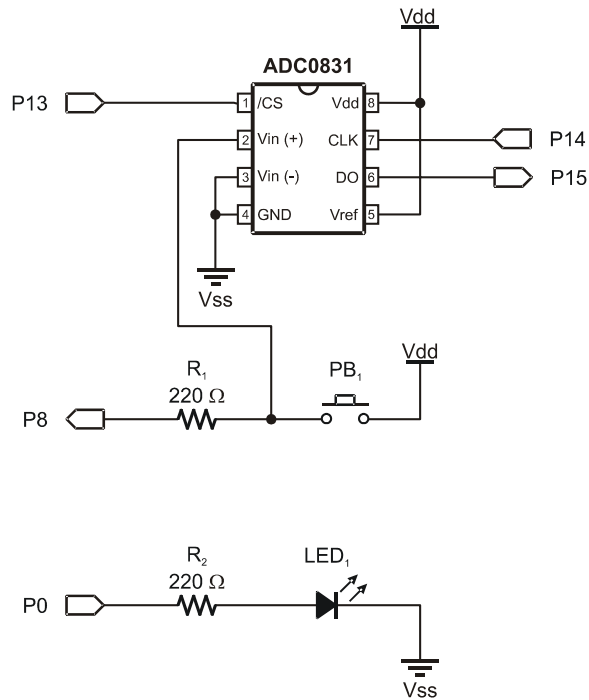
Figure 3-6
Uncommitted
Pushbutton

√   Monitor the digital and analog values.
√   Momentarily touch the lead of R_1 on the pushbutton side. What occurs? (Results may vary depending on conditions.) Try rubbing your hair first to build up a static charge on your hand.
√   Press the pushbutton while momentarily touching the lead. What occurs?

Figure 3-7 is a sample plot of the results.
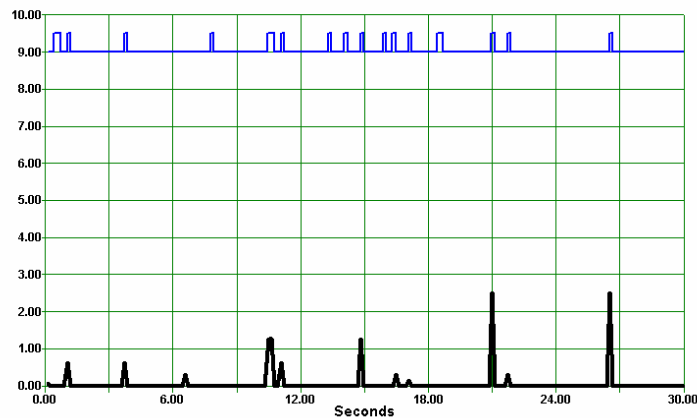
Figure 3-7
Plot of
Uncommitted
Input

When the pushbutton is pressed, current passes through the switch to register a solid HIGH value. The input is now committed and no longer floating.

When the normally-open (N.O.) pushbutton is not pressed, the input to P8 is floating and not committed to any voltage level. By touching the lead, the static electricity on your body is creating voltage spikes on the input above the threshold voltage. This noise causes the digital input to switch states. During process control, the uncommitted input may cause erratic and undesirable conditions. Again, the monitored analog voltage and digital input are not measured simultaneously and may not match HIGH and LOW values exactly.

√ Place a 10 kΩ resistor from the P8 side of the pushbutton to Vss as shown in Figure 3-8.
√ Test the circuit again. Are the results more stable?
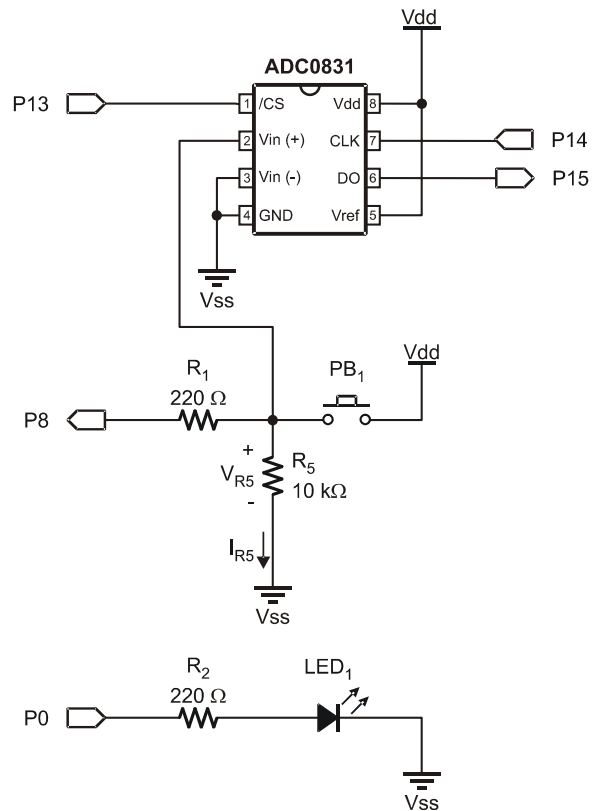
Figure 3-8
Active-High
Pushbutton with Pull-
Down Resistor

The pull-down resistor R_5 is used to force the input to a low voltage when the pushbutton is not pressed, keeping it LOW. When the button is pressed, current flows through R_5, allowing a HIGH to be sensed on P8. The pull-down resistor should be sized to prevent excessive current flow when the button is pressed.

$$I_{R5}=V_{R5}/R_5 = 5 \text{ V}/10 \text{ k}\Omega = 0.5 \text{ mA}$$

Typical values for resistors used for this purpose are 1 kΩ, 10 kΩ or even 100 kΩ. A minimum amount of current is required, typically several microamps.

The pushbutton circuit is termed Active-High because when the button is active (pressed), the input state will be HIGH, a pull-down resistor is used to force the input LOW (when the pushbutton is not pressed).

> **Always check data sheets for the digital device in use.** Different devices have different input voltage and current specifications. They may be damaged by static electricity when inputs are left uncommitted. Some devices may have internal pull-up resistors, alleviating the need of adding them to the input. TTL devices will typically assume a HIGH state if not connected, but this is not assured, especially during internal clocking or switching.

Challenge 3-3: Active-Low Pushbutton Circuit

Consider the circuit in Figure 3-9.

1. This circuit is termed Active-Low. Why?
2. Does this circuit use a Pull-Up or Pull-Down resistor? Why?
3. Reconfigure your circuit to match, and test. Discuss your results.
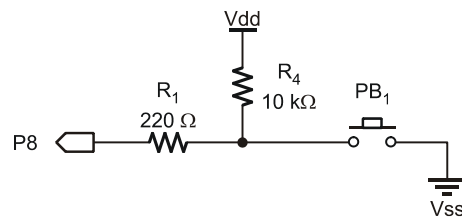
Figure 3-9
Active-Low
Pushbutton Circuit

## ACTIVITY #4: THE TRANSISTOR AS A SWITCH

The transistor revolutionized electronics and is the basic building block in both analog and digital systems today. The Bipolar Junction Transistor (BJT) can be used as an amplifier to take a small analog signal, such as sound waves hitting a microphone, and amplifying that signal many times to be blasted out by speakers at rock concerts.

The transistor may also be used as a digital switch – ON or OFF. The BASIC Stamp and the microprocessor that runs your computer system are two examples of thousands, or

millions, of transistors working together as an Integrated Circuit (IC) to perform sophisticated operations.

As a switch, the transistor may be driven to a condition where it drops virtually no voltage and allows full current flow in a load. In this condition, it acts similar to a closed switch. No drive control applied to the transistor causes it to behave like an open switch. The transistor is semi-conductor configured to control current flow, allowing it to be fully on, fully off, or anywhere in between.

Figure 3-10 represents a typical discrete transistor. A BJT has 3 leads: Base (B), Emitter (E) and Collector (C). This transistor symbol tells us that it is an NPN.

I_B

I_C

C

B

E
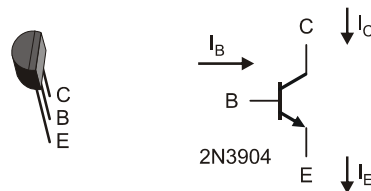
2N3904

Figure 3-10
2N3904 NPN Transistor

I_E

The BJT is a current-controlled device. A small base-current (I_B) is used to control a much larger collector-current (I_C). I_B controls I_C.

The transistor has 3 operating regions and can be thought of as a water valve. When the valve (the base) is off, there will be no water flow in the pipe (collector-emitter). As you begin opening the valve, the amount of water flowing in the pipe is proportional to how far the valve is opened. At a certain point, opening the valve any further may not produce any appreciable change in water flow. Restrictions in the pipe and supply water pressure limit the flow rate.

There are three operating regions of the transistor as shown in Figure 3-11.

- Cutoff Region: Insufficient voltage on the base to produce appreciable current flow in the base and, therefore, no collector current. As an electronic switch, the collector to emitter is "open" and collector-current (I_C) is essentially zero.

- Active Region: The amount of current flow in the collector is directly proportional to the current flow in the base. The BJT is somewhere between fully-off and fully-on, controlling current flow. I_C is equal to the base-current

3

(I_B) multiplied by a gain factor called Beta (β) or, when dealing with strictly DC values, h_{FE}.

$I_C = I_B$ x h_{FE}.

- Saturation Region: An increase in base current does not change the collector current. The electronic switch is closed. Resistance in the collector-emitter circuit limits I_C. The transistor is in saturation, and the collector current is termed saturation current (I_{SAT}).
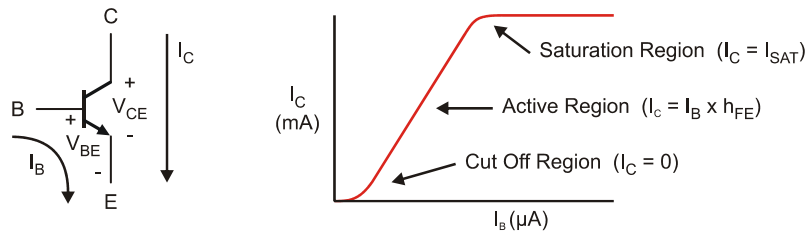
---

i

In keeping with Kirchoff's Currrent Law (KCL) which states that the algebraic sum of the currents entering any node is zero:

$I_B + I_C - I_E = 0$

$I_E = I_B + I_C$

Figure 3-11 Transistor Current Flow and Characteristic Curve

All devices have limits and specifications for proper operation. Table 3-1 shows the pertinent specifications for the 2N3904. Some specifications are characteristics of the device, such as the voltage drop at the base-emitter junction (denoted by "Device" in the table). For example, the Collector to Emitter voltage drop is typically 0.3 V when current is flowing.

Other specifications are limitations imposed on the user to prevent damage to the device (denoted by "Use" in the table). For example, the maximum supply voltage to the device.

Table 3-1: 2N3904 Transistor Specifications		
Parameter	**Value**	**Meaning**
h_{FE} or ß	100 – 300	Current Gain I_C/I_B (Device)
I_C	200 mA	Maximum Collector Current Continuous (Use)
V_{CE}	0.3 V	Voltage dropped Collector-Emitter when in saturation (Device)
V_{BE}	0.65 V – 0.95 V	Voltage across Base-Emitter junction (Device)
V_{ECO}	40 V	Maximum Voltage Collector-Emitter (Use)
P_D	625 mW	Maximum Power Dissipation (Use)

Let's perform testing and calculations for a simple transistor circuit.

Parts Required

(1) ADC0831
(2) Resistors – 220 Ω
(1) Resistor – 1 kΩ
(1) Resistor – 47 kΩ
(1) Potentiometer – 10 kΩ
(1) Transistor – 2N3904
(1) LED – Red

√   Construct the circuit shown in Figure 3-12.
√   Run the program DataMonitoring.bs2
√   Close the Debug Terminal.
√   Run StampPlot macro sic_pc_data_monitoring.spm.
√   Connect and plot.
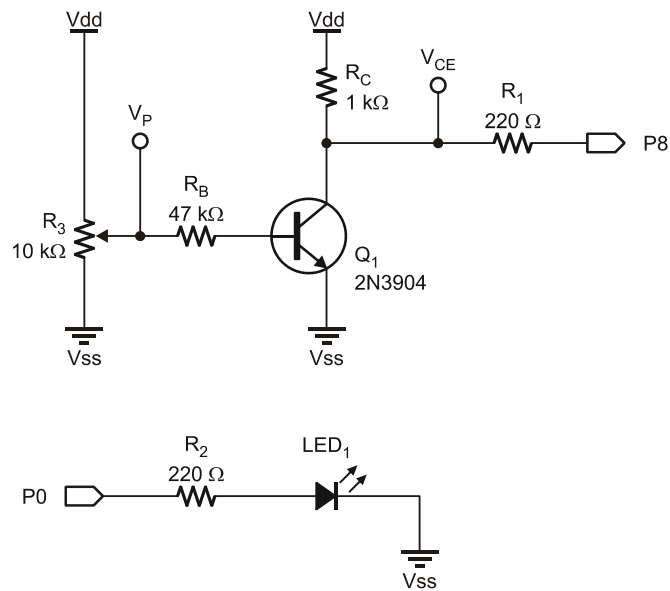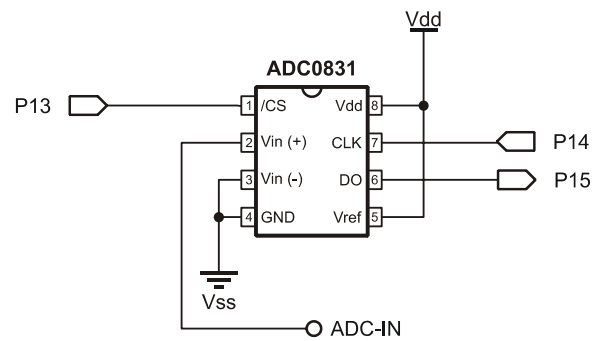
Figure 3-12
Transistor
Monitoring
Circuit

√ Connect ADC-IN to V_P. Adjust the potentiometer and note the direction that causes an increase in voltage (clockwise or counterclockwise).

√ Disconnect ADC-IN from V_P, and connect it to V_{CE}. What occurs as the potentiometer is adjusted? Does the increase in voltage follow V_P, or is it just

the opposite of it? Does the voltage at V_{CE} change over the full movement of the potentiometer or only over a portion of movement?

Analyzing what is occurring with reference to Figure 3-13:

- As V_P increases in voltage, the current through the base (I_B) increases.
- I_B increasing leads to increased current in the collector (I_C).
- As I_C is increased, more voltage is dropped across the collector resistor R_C.

$$V_{RC} = I_C R_C$$

- The voltage drop across the transistor Collector to Emitter (V_{CE}) must decrease.

$$V_{CE} = 5\ V - V_{RC}$$

- So, as V_p increases, V_{CE} decreases over a certain range.

As the potentiometer is adjusted from minimum to maximum, the transistor goes from cutoff through the active region to saturation.
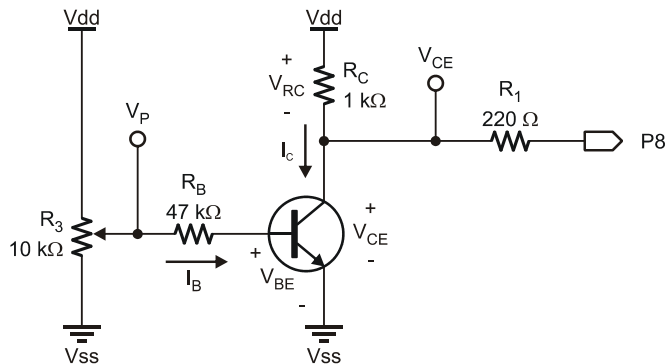
Figure 3-13

Voltage and Current Characteristics

Cutoff Region:

With insufficient base current, the transistor will essentially be off (an open switch) and acts as a very high resistance from collector to emitter. I_C will be zero, and the voltage at the output (V_{CE}) will be supply voltage, or Vdd in this case. This is also known as V_{CUTOFF}.

Linear Region:

In the linear region, the collector current, (I_C), is a function of the base-current multiplied by the DC gain of the transistor, h_{FE}. The 2N3904 can have a gain of 100 to 300. V_{CE} is a function of the current flow, creating a voltage drop across R_C. For example, given: $h_{FE} = 200$, $I_B = 10$ μA, and a 5 V supply; calculate I_C, V_{RC} and V_{CE}.

$$I_C = I_B\, h_{FE} = (10\ \mu A)(200) = 2000\ \mu A = 2\ mA.$$
$$V_{RC} = I_C\, R_C = (2\ mA)(1\ k\Omega) = 2\ V$$
$$V_{CE} = Vdd - V_{RC} = 5\ V - 2\ V = 3\ V$$

> **Ⓘ**   **Vcc vs. Vdd**   Officially, the collector voltage is called Vcc when working with BJTs which have a collector. Vdd is more properly used with Field Effect Transistors (FET) which have a drain instead of a collector. The BASIC Stamp is constructed with FETs, thus the Vdd designation is used.

What if I_B were 100 μA? What do the calculations show for I_C, V_{RC} and V_{CE}?

$$I_C = I_B\, h_{FE} = (100\ \mu A)(200) = 20000\ \mu A = 20\ mA.$$
$$V_{RC} = I_C\, R_C = (20\ mA)(1\ k\Omega) = 20\ V$$
$$V_{CE} = Vdd - V_{RC} = 5\ V - 20\ V = -15\ V$$

Does this make sense? How did we get 20 V across R_C with a supply of 5 V? The transistor had long gone into saturation when V_{CE} went down to 0 V and all of Vdd was applied across R_C.

Saturation Region:

As shown, there must be some limit to how much current can be developed in the collector. The current limit is based on the supply voltage and the value of R_C and is called saturation current (I_{SAT}).

$$I_{SAT} = Vdd/R_C = 5 \text{ V}/1 \text{ k}\Omega = 5 \text{ mA}.$$

At saturation, when the transistor is in full conduction, V_{CE} will be at the minimum, and the transistor will be conducting as much collector current as possible based on the restriction of R_C (fully-on or acting as a closed switch). At saturation, the collector to emitter junction of the transistor will always drop a small amount of voltage, typically 0.3 V. Therefore, I_{SAT} will be slightly less.

$$I_{SAT} = (Vdd - 0.3 \text{ V})/R_C = 4.7 \text{ V}/1 \text{ k}\Omega = 4.77 \text{ mA}$$

Over a current range of 0 mA to 4.77 mA, the transistor will be in the active region. With an h_{FE} of 200, control is defined over a range of 0 mA to 23.5 µA for I_B.

$$I_B = I_C/h_{FE} = 4.77 \text{ mA}/200 = 23.5 \text{ µA}$$

Any base current above this value will cause the transistor to be in saturation and at maximum current.

Consider an increase in the value of R_C to 10 kΩ. Based on a 5 V supply, with an h_{FE} of 200, calculate values for I_{SAT} and I_B at saturation.

$$I_{SAT} = (Vdd - 0.3 \text{ V})/R_C = 4.7 \text{ V}/10 \text{ k}\Omega = 0.477 \text{ mA}$$
$$I_B = I_C/h_{FE} = 0.477 \text{ mA}/200 = 2.35 \text{ µA}$$

Would the potentiometer require more or less voltage to drive the transistor into saturation? Since 10 times less current is required, 10 times less voltage is required at the base to drive the transistor into saturation.

Transistor Power Dissipation

Power is the work performed by a device or system per unit of time. In electronics power is measured in watts. Light bulbs are devices we commonly purchase based on the power output, such as 60 watt, 100 watt or even 200 watt bulbs. A light bulb's power is in the

amount of light that is produced (lumens) as well as the heat produced and dissipated to the air around it. Any device that has current flowing through it and a voltage drop across it coverts electricity into power. This power may be useful work (light, motion) or heat to be dissipated – which could also be useful at times, such as your clothes dryer.

> **ⓘ** **DC Power Dissipation**: The power dissipated by an element in a DC circuit is given by the voltage across the element multiplied by the current flowing through it:
>
> **Power = Voltage x Current**
>
> **P = VI**

When the power takes the form of heat, it must be dissipated from the device either by convection to the air or through other means. The CPU in your computer system consumes a large amount of power, and if the heat is not removed, damage to the CPU will quickly occur. Heat sinks provide heat conduction from the device, a greater area of cooling and often fans are added for forced convection to remove heat more efficiently.

Transistors, such as the ones in your CPU, have current flowing through them and have a voltage drop across them. Since a transistor operates in 3 distinct areas, when is the most power consumed?

- When in cutoff, the voltage drop is at maximum (V_{CUTOFF}), but current flow is minimum (theoretically 0).
- When in saturation, the current flow is at maximum (I_{SAT}) but the voltage drop is minimum (0.3 V).

Maximum power is used by the transistor when it is mid-point biased where V_{CE} is ½ V_{CUTOFF} and current is ½ I_{SAT} (these occur at the same time).

$$P_{Q1\ Max} = \tfrac{1}{2}\ (Vdd)\ \text{x}\ \tfrac{1}{2}\ (I_{SAT})$$

For our circuit, the highest power can be calculated:

$$Vdd = 5\ V,\ I_{SAT} = 5\ mA$$
$$P_{Q1\ Max} = (0.5\ )(5\ V)\ \text{x}\ (0.5)(5\ mA) = 6.25\ mW$$

The maximum power that the 2N3904 can dissipate (P_D) is 200 mW without adding heat sinks and fans. We are well within the device's specifications.

Keep in mind that when using the transistor as a switch (in saturation or cutoff), the maximum power occurs only during the transition so that the power dissipated will be very low. The more frequently the transition occurs (frequency), the more the transistor is passing through the active region; therefore, the higher the average power that is being dissipated.

Challenge 3-4: Calculating Current and Power

Given a 2N3904 transistor with a collector supply voltage of 40 V and R_C of 500 Ω, calculate I_{SAT} and $P_{Q1\ MAX}$. Is there a concern based on power consumption and heat generation?

ACTIVITY #5: EFFECTS OF RESISTOR SIZING

R_C size plays a big role in the circuit by defining I_{SAT} and power. It also plays a role in the response of the circuit, how quickly it can respond to input changes.

Parts Required

Circuit from Activity #4
(1) Resistor – 10 kΩ

   √   Begin with the circuit from Activity 3, Figure 3-12 with ADC-IN connected to V_{CE}.
   √   Run the program DataMonitoring.bs2.
   √   Run the StampPlot macro sic_pc_load_line.spm.
   √   Connect and plot.
   √   Adjust the potentiometer slowly between its minimum and maximum values.

StampPlot calculates and plots the DC Load Line for this value of R_C (1 kΩ). You can see a sample image in Figure 3-14.

The Load Line is a graphical representation of V_{CE} to I_C over the linear region. Note that when in cutoff, V_{CE} is at the supply voltage of 5 V. When in saturation, I_C is at maximum, based on the size of R_C and Vdd. Furthermore, based on I_C and V_{CE}, the power of the transistor (P_{Q1}) is plotted. Note the shape of the curves and when power is the maximum.

Figure 3-14 DC Load Line and Transistor Power
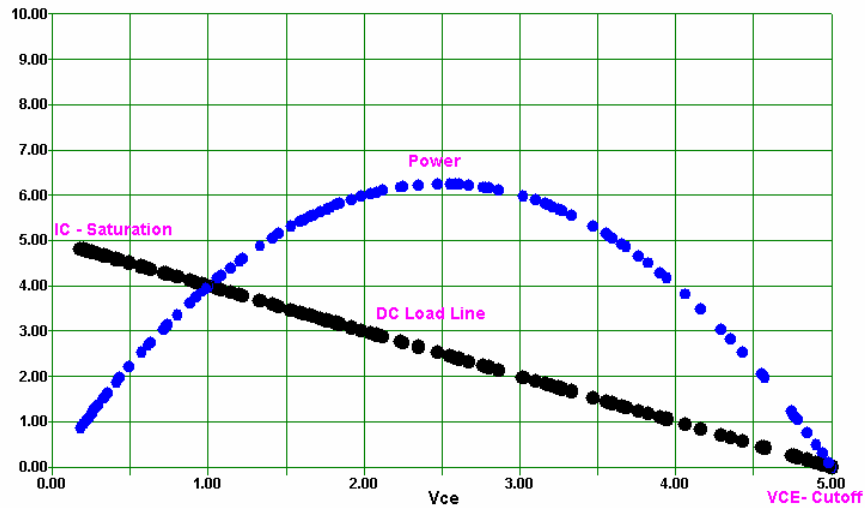
- √ Adjust the potentiometer slowly. Note the range over which the load line goes from cutoff to saturation.
- √ Replace R_C with a 10 kΩ resistor.
- √ In StampPlot, change the value of R_C to 10.
- √ Adjust the potentiometer slowly over its full range.

What happens to the load line? The value of I_{SAT} is smaller by a factor of 10. Power is reduced by a factor of 10 also.

Relative to using a 1 kΩ value for R_C (see Figure 3-12 and Figure 3-13), how much movement does it now take to control the transistor over its full active range? Since I_{SAT} is so much smaller, a much lower value of I_B required for saturation is defined, and thus a much lower value of V_P to reach saturation, which means the potentiometer needs to be rotated a smaller amount.

- √ Return R_C to a value of 1 kΩ.
- √ Change StampPlot RC value to 1.

√   Reset the plot and re-acquaint yourself with the results of movement for the potentiometer.
√   Replace R_B with the 10 kΩ resistor.
√   Reset the plot and adjust the potentiometer very slowly to obtain a new plot.

Has the load line for the 1 kΩ resistor changed? How much movement of the potentiometer is required over the full active region as compared to the 47 kΩ? When R_B is reduced, the base current is higher for the same voltages. Because I_B is higher, I_C is higher over a smaller movement range of the potentiometer.

√   Return R_B to a value of 47 kΩ.

Challenge 3-5: Considerations for a Transistor Switch

1. If the transistor were being used as a digital switch, would a higher or lower value of R_C be desirable based on the DC Load Line and input voltage response? Why?

2. What would the DC Load Line look like if a 100 kΩ resistor were used for R_C? Draw a plot of the Load Line and Power. Scale the plot accordingly for readability.

Other Considerations in Sizing Resistors

While it may appear that a high value of R_C is desirable for switching action of a transistor, this is not necessarily the case. The switching speed of the circuit is faster as the value of R_C decreases. The data sheets for the 2N3904 can lend credence to this. In later chapters we will see this in action. Figure 3-15 is a characteristic curve of rise time (t_r) vs. I_C.

As I_C increases (lower R_C), the rise time of the transistor decreases. This is approximately the time required to go from cutoff to saturation. The lower the rise time value, the faster the transistor can go from cutoff to saturation and vice-versa. Increasing R_C leads to increased sensitivity but slower switching.

Rise Time vs Collector Current

$V_{cc} = 40V \quad I_B = I_{B2} = \dfrac{I_C}{10}$
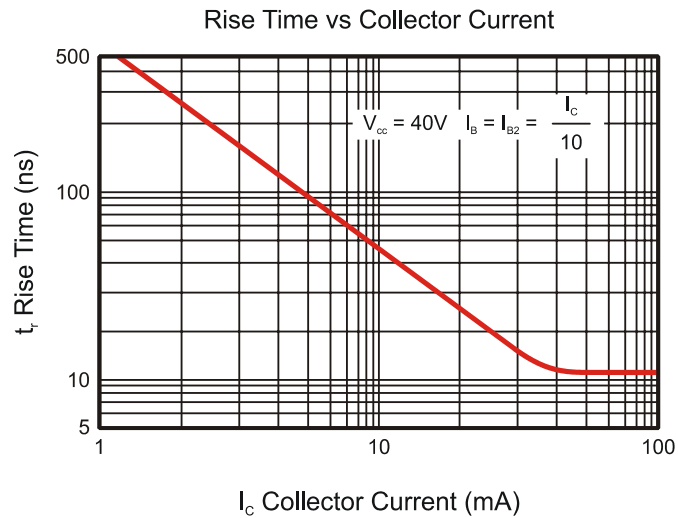
Figure 3-15
2N3904 Transistor
Characteristic Curve

Another effect is loading on the output. Take, for example, a voltmeter with an input impedance of 1 MΩ. If R_C is 1 MΩ and the transistor is in cutoff, what voltage will be read? It should be 5 V since the transistor is in cutoff, but R_C of the output and the meter input form a voltage divider as shown in Figure 3-16. The actual measured voltage would be 2.5 V. This is termed "loading".
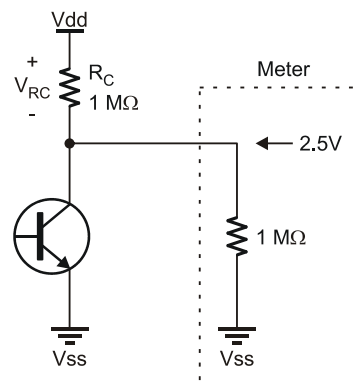
Figure 3-16
Loading Effects

> ℹ **Impedance** is similar to resistance, but also takes into account AC characteristics, which will not be explored in this text.

Ideally, the output impedance of a device should be zero, and the input impedance should be infinite to transfer the maximum voltage. Since we don't live in an ideal world, the input impedance should be at least 10 times the value of the output impedance between devices so that loading effects are not an issue. For example, if the input impedance of a device is 1 MΩ, the output impedance of the device supplying it should be no more than 100 kΩ.

Using the transistor as an input from another device, a higher base resistance is desirable to prevent loading and excessive current from the supplying device. Note that the control of the transistor is dependent on base current. As long as R_B is sized properly, this voltage may be smaller or larger than Vdd. This allows a means to interface devices operating at different supply voltages.

ACTIVITY #6: SWITCHING CONFIGURATION COMPARISONS

Figure 3-17 is a comparison of an Active-Low pushbutton switch and the common-emitter transistor circuit that we have been using.

Figure 3-17 Switch Equivalent Common-Emitter Configuration

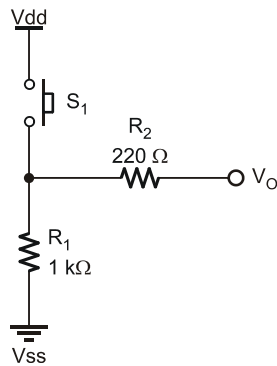*N. O. Active Low Switch with Pull-up*   *Common-Emitter Configuration*
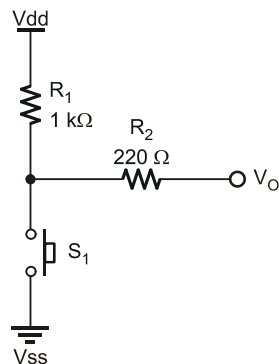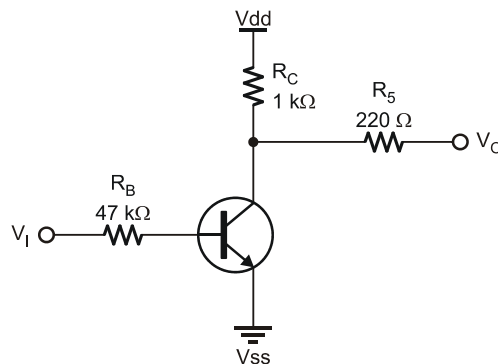
Note the similarities in operation:

- The pushbutton is activated by pressing it. The transistor is active (in saturation) when sufficient voltage is applied to V_I providing the base current required.
- Both circuits have a HIGH output when the switch is not active through the use of pull-up resistors.
- Both outputs go LOW when the device is activated.

Another transistor configuration is the common-collector. What is common (emitter, collector, or base) can be recognized by which terminal is NOT used by either the input or the output. Consider the comparison in Figure 3-18 to a pushbutton switch.

Figure 3-18 Switch Equivalent Common-Collector Configuration

N. O. Active High Switch with Pull-down   *Common-Collector Configuration*
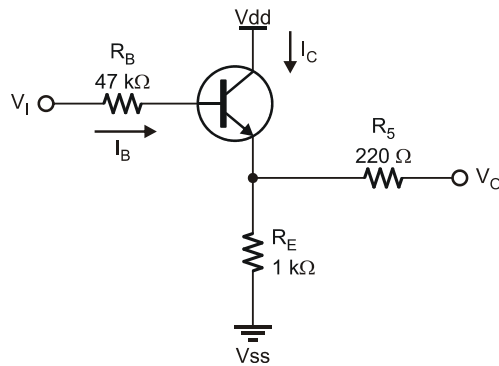
The transistor will be in cutoff and act as an open-switch when insufficient V_I is applied to the transistor base. Just as with the pushbutton the output will be LOW through the pull-down resistor.

When V_I is a sufficient voltage, the base current will drive the transistor into saturation, acting as a closed-switch and Vdd will be felt on the output (minus 0.3 V dropped across the collector-emitter junction).

The common-collector is slightly more difficult to analyze, and we will only briefly discuss it. In the common-emitter the base current is calculated through:

$$I_B = (V_I - 0.7)/R_B$$

The collector current is determined from this value using h_{FE}.

$$I_C = I_B \, h_{FE}$$

In the common-collector, what determines the base current? Both R_B and R_E are in series from Vss to V_I, so a quick assumption would be $R_B + R_E$. But this is not correct because R_E lies on the emitter side, so the effects of h_{FE} must be considered. From the base's perspective, R_E is not 1 kΩ for this circuit but h_{FE} x R_E.

$$I_B = (V_I - 0.7 \text{ V})/(R_E \, h_{FE} + R_B)$$

Reducing the value of R_B to zero with a Vin of 5 V there may be insufficient base current to drive the transistor into saturation current. I_{SAT} is defined by Vdd/R_E in this configuration. Assuming $h_{FE} = 100$:

$$I_B = (V_I - 0.7)/(h_{FE} \, R_E + R_B)$$
$$I_B = (5 \text{ V} - 0.7)/((100)(1 \text{ k}\Omega) + 0) = .043 \text{ mA}$$

$$I_C = I_B \, h_{FE} = 4.3 \text{ mA}$$

$$I_{SAT} = (Vdd - 0.3)/R_E$$
$$I_{SAT} = (5 \text{ V} - 0.3 \text{ V})/ 1 \text{ k}\Omega = 4.7 \text{ mA}$$

With a V_I of 5 V and no R_B, I_C is almost at I_{SAT}, but not quite.

Challenge 3-6: Decreasing R$_E$ in the Common-Collector Configuration

If R_E is decreases to 100 Ω, will a 5 V Vin and R_B of 47 kΩ be able to drive the transistor into saturation?

ACTIVITY #7: TYPICAL INDUSTRIAL SWITCHES

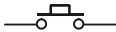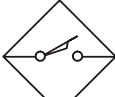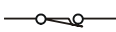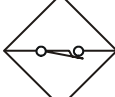The pushbutton is just one of many switches available. Figure 3-19, Figure 3-20, and Table 3-2 show a variety of different switches commonly used in industrial applications. These switches may be either mechanical or electronic in their operation.

A mechanical switch, such as the pushbutton, opens or closes contacts to allow current to flow. When being used as an input to the BASIC Stamp, a pull-up or pull-down resistor is needed. The need for output conditioning is true of many electronic switches as well.

Electronic switches that provide "non-contact" detection are very popular in industrial applications. No physical contact for actuation means no moving parts and no electrical contacts to wear out. The pushbutton switch used earlier should be good for several thousand presses. However, its return spring will eventually fatigue, or its contacts will arc, oxidize, or wear to the point of being unreliable.

Figure 3-19
Different
Switches used
in Industry

Table 3-2: Schematic Symbols for Various Industrial Switches

|	Pushbutton	Mechanical Limit	Proximity Switch	Relay Contacts
Normally Open				
Normally Closed				

The proximity switches shown in Figure 3-20 are commonly used in industry to detect the presence of an object and operate on one of three principles:

- Inductive proximity switches sense a change in an oscillator's performance when metal objects are brought near. Most often, the metal objects absorb energy via eddy currents from the oscillator, causing it to stop.

- Capacitive proximity switches sense an increase in capacitance when any type of material is brought near. When the increase becomes enough, it causes the switch's internal oscillator to start oscillating. Circuitry is then triggered, and the output state is switched.

- Optical switches detect the presence or absence of a narrow light beam, often in the infrared range. In retro-reflective optical switches, an object moving into the switch's range may reflect the light beam back to the sensor. Through-beam optical switches are set up such that the object blocks the light beam going between the light source and the receiver.

Figure 3-20
Inductive, Capacitive
and Optical Proximity
Switches

A common final output stage of an electronic switch is shown in Figure 3-21.
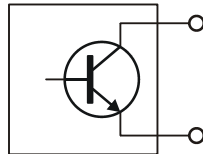
Figure 3-21
Typical Electronic
Switch Output

This configuration allows maximum flexibility for engineers in integrating it into their systems. The output may be configured as common-emitter or common-collector, and the resistors sized appropriately.

Other devices may simply output a digital HIGH and LOW. If the device does not use the same supply, ensure that output voltages are compatible with the BASIC Stamp. If the switch is powered from another supply, the grounds will need to be connected together. Figure 3-22 and Figure 3-23 illustrate various methods of interfacing digital devices.

Vdd

Any TTL
Output

+5V Logic O

BS2 Input

Vss
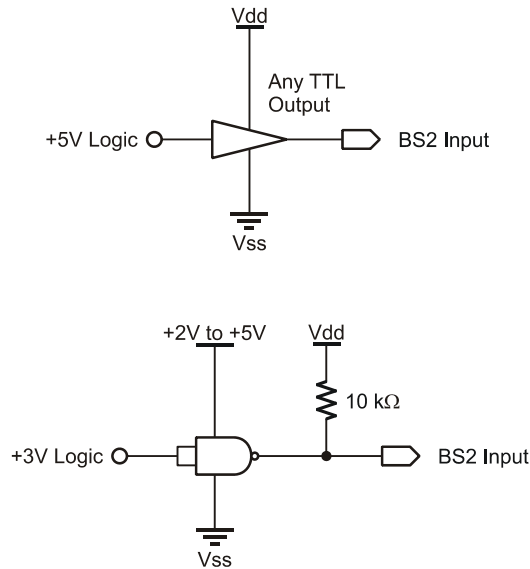
Figure 3-22
Digital Interface
Circuits

*Top: Standard TTL
to BASIC Stamp*

+2V to +5V   Vdd

10 kΩ

+3V Logic O

BS2 Input

Vss

*Bottom: Low Voltage
Logic to BASIC
Stamp*

Figure 3-22 (top): TTL and CMOS logic inputs powered from a +5 volt supply can be applied directly to the BASIC Stamp input pins. If the two systems are supplied from the same 5 volts, great. If not, at least the grounds must be common (connected together).

Figure 3-22 (bottom): Low-voltage (+3 V) devices can be interfaced using a 74HCT03, or similar open-drain devices, with a pull-up resistor to the BASIC Stamp module's +5 volt supply. Supply the chip with the low-voltage supply and make the grounds common.

3
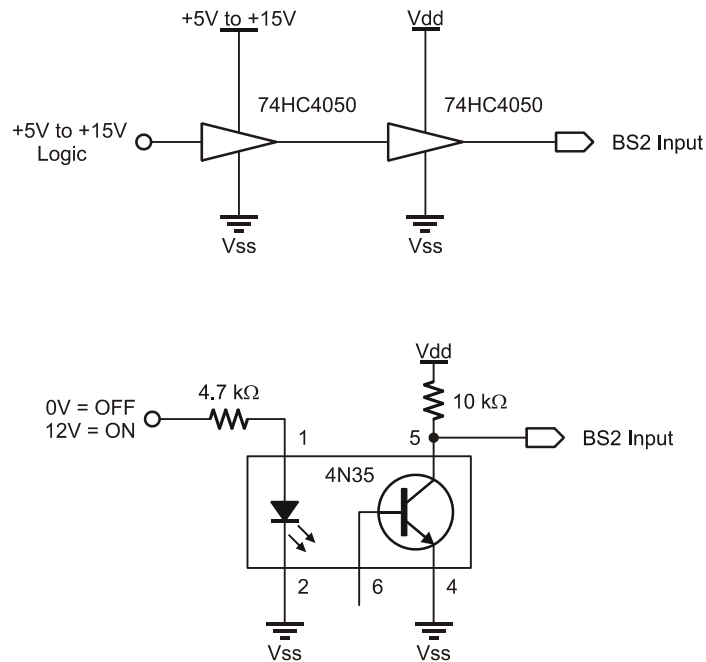
Figure 3-23
Digital Interface
Circuits

*Top: High
Voltage Logic to
BASIC Stamp*

*Bottom:
Optocoupler to
BASIC Stamp*

Figure 3-23 (top): Higher-voltage digital signals can be interfaced using a 74HC4050 buffer or 74HC4049 inverter powered at +5 volts. These devices can safely handle inputs up to 15 volts. Again, the grounds must be common.

Figure 3-23 (bottom): An opto-coupler may be used to interface different voltage levels to the BASIC Stamp. The LED's resistor holds current to a safe level while allowing enough light to saturate the phototransistor. The input circuit can be totally isolated from the phototransistor's BASIC Stamp power supply because they do not need to share a common-ground. This isolation provides effective protection of each circuit in case of an electrical failure of the other.

The optical reflective switch will be explored further in Chapter 4.

Challenge 3-7: Wiring a Relay

The relay can use high voltage, AC or DC, to energize a solenoid that closes or opens electrically isolated mechanical contacts that can be used as input to the BASIC Stamp. Signal conditioning these contacts is similar to the use of pull-up or pull-down resistors.

√   Wire the contacts (by drawing) in Figure 3-20 so the BASIC Stamp senses a HIGH when S1 is closed, which energizes the solenoid and magnetically opens the normally closed relay contacts labeled K1.
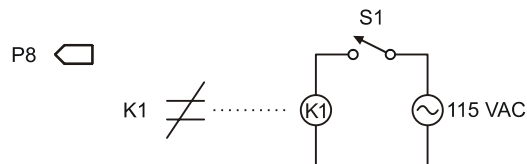
Figure 3-24
Sensing 115 V with a Relay

(Drawing to be completed by student – do not build)

CONCLUSION

When acting as inputs, the BASIC Stamp typically senses a digital HIGH value for any voltage above approximately 1.4 V and a digital LOW below 1.4 V. An input to the BASIC Stamp does not necessarily need to be 5 V or 0 V, but must at least cross this threshold voltage. Input voltages above 6 V will damage the BASIC Stamp.

BASIC Stamp inputs are uncommitted. That is, they are neither HIGH nor LOW without an input committing them to the positive voltage or down to ground respectively. Most mechanical switches require a pull-up or pull-down resistor for an Active-Low or Active-High configuration respectively. Mechanical and electronic switches often require proper conditioning.

Bipolar Junction Transistors (BJT) are current controlled devices that can operate as current amplifiers or electronic switches. The base current controls the current in the collector. With no base current, the transistor will be cutoff and act as an open switch. With sufficient base current, the transistor's collector current will be at saturation, and the transistor will act as a closed switch. The saturation current is a function of the supply

voltage and the resistance of the collector for the configuration studied. The DC Load Line is a graphical representation of output voltage and collector current over the linear range.

The value of R_C in a common-emitter configuration determines the saturation current, and thus, the base current required to drive the BJT into saturation. The higher the value of R_C the more sensitive the transistor will be to base current. But high values of R_C also limit response and switching speeds of the transistor. The maximum power dissipated by the transistor occurs when it is conducting ½ of saturation current, which leads to heating.

SOLUTIONS TO CHAPTER 3 CHALLENGES

Challenge 3-1 Solution

When the potentiometer supply leads are reversed, rotation will result in the opposite direction of voltage change as compared to previously. For example, when rotated clockwise, the wiper of the potentiometer will be closer to Vdd as opposed to Vss previously.
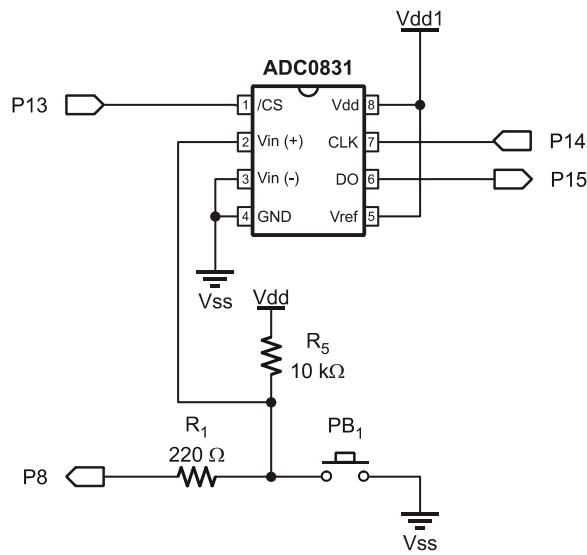
Challenge 3-2 Solution

Placing the photoresistor on the Vdd side of the potentiometer modifies the circuit for a darkroom sensor. When more light falls on it, the resistance decreases dropping more voltage across the bottom half causing voltage to increase. The potentiometer must again be adjusted for the desired light/dark threshold in the darkroom.
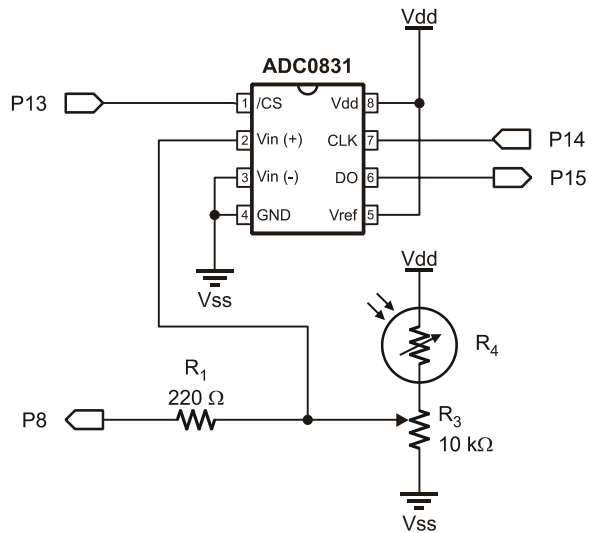
Figure 3-25
Photographic Darkroom Alarm
Circuit Solution

Challenge 3-3 Solution

1. The circuit in the figure is termed Active-Low because when the button is pressed (active) a connection is made to Vdd.
2. A pull-up resistor used to keep the input high (up = high) when the switch is not active.
3. Your circuit should look like Figure 3-26. Pressing the button after reconfiguring should have caused the digital plot to go low.

Figure 3-26
Active-Low
Pushbutton Solution

Challenge 3-4 Solution

$I_{SAT} = (40\text{ V}- 0.3\text{ V})/500\Omega = 79.4$ mA

Maximum continuous is 200 mA, so OK.

$P_{Q1\ MAX} = $ ½ I_{SAT} x ½ $V_{dd} = (0.5)(79.4$ mA$)$ x $(0.5)(40$ V$) = 794$ mW

Maximum is 625 mW so heat sinking is required.

Challenge 3-5 Solution

1. A higher value of R_C is desirable based on the response to the input (sensitivity). Lower I_B is required, therefore less in change of V_{IN} and shorter time spent in linear region in going from saturation to cutoff.
2. $I_{SAT} = (Vdd − 0.3)/R_C = 4.7$ V/100 k$\Omega = 0.047$ mA
$P_{Q1\ MAX} = $ ½ I_{SAT} x ½ $V_{dd} = (0.5)(0.047$ mA$)$ x $(0.5)(5$ V$) = .1175$ mW

Load line would go to 0.047 on Y-axis to 5 V (cutoff) on X-axis.

Challenge 3-6 Solution

$I_B = (V_I - 0.7)/(h_{FE} R_E + R_B)$
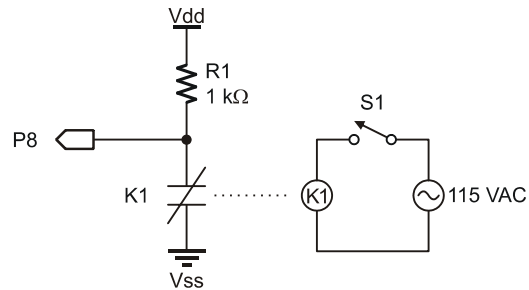$I_B = (5\ V - 0.7)/((100)(100\ \Omega) + 47\ k\Omega) = 0.075\ mA$

$I_C = I_B \times h_{FE} = (0.075\ mA)(100) = 7.5\ mA$

$I_{SAT} = (Vdd - 0.3)/R_E$
$I_{SAT} = (5\ V - 0.3\ V)/100\ \Omega = 4.7\ mA$

$I_C > I_{SAT}$. Saturation current can be reached.

Challenge 3-7 Solution

- When S1 is open, the relay is de-energized and contacts K1 are closed. P8 senses LOW.
- When S1 is closed, the relay is energized and contacts K1 open. P8 senses HIGH.

Figure 3-27
Completed Drawing

Do Not Build