Precision Instrumentation Amplifier

AD524

FEATURES

Low noise: 0.3 µV p-p at 0.1 Hz to 10 Hz
Low nonlinearity: 0.003% (G = 1)
High CMRR: 120 dB (G = 1000)
Low offset voltage: 50 µV
Low offset voltage drift: 0.5 µV/°C
Gain bandwidth product: 25 MHz
Pin programmable gains of 1, 10, 100, 1000
Input protection, power-on/power-off
No external components required
Internally compensated
MIL-STD-883B and chips available
16-lead ceramic DIP and SOIC packages and 20-terminal leadless chip carrier available
Available in tape and reel in accordance with EIA-481A standard
Standard military drawing also available

FUNCTIONAL BLOCK DIAGRAM

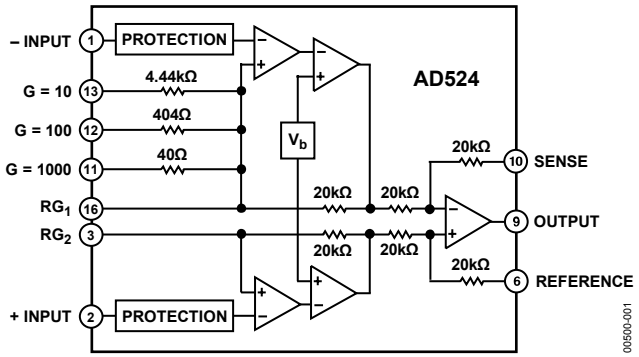

Figure 1.

GENERAL DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common-mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25 µV/°C, input offset voltage drift of less than 0.5 µV/°C, CMR above 90 dB at unity gain (120 dB at G = 1000), and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications, the AD524 also has a 25 kHz bandwidth (G = 1000). To make it suitable for high speed data acquisition systems, the AD524 has an output slew rate of 5 V/µs and settles in 15 µs to 0.01% for gains of 1 to 100.

As a complete amplifier, the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1000. For other gain settings between 1 and 1000, only a single resistor is required. The AD524 input is fully protected for both power-on and power-off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical A grade, the low drift B grade, and lower drift, higher linearity C grade are specified from −25°C to +85°C. The S grade guarantees performance to specification over the extended temperature range −55°C to +125°C. The AD524 is available in a 16-lead ceramic DIP, 16-lead SBDIP, 16-lead SOIC wide packages, and 20-terminal leadless chip carrier.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift, and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100, and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power-on and power-off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25 MHz, full power response of 75 kHz and a settling time of 15 µs to 0.01% of a 20 V step (G = 100).

Rev. F

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Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is the component of offset that is directly proportional to gain, that is, input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, at high gains, input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), whereas input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input related numbers are referred to the input (RTI) that is the effect on the output is G times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formulas:

Total error RTI = input error + (output error/gain)

Total error RTO = (gain × input error) + output error

As an illustration, a typical AD524 might have a +250 µV output offset and a −50 µV input offset. In a unity gain configuration, the total output offset would be 200 µV or the sum of the two. At a gain of 100, the output offset would be −4.75 mV or: +250 µV + 100(−50 µV) = −4.75 mV.

The AD524 provides for both input and output offset adjustment. This simplifies very high precision applications and minimizes offset voltage changes in switched gain applications. In such applications, the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gains of 1, 10, 100, and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together (for G = 1, RG_2 is not connected).

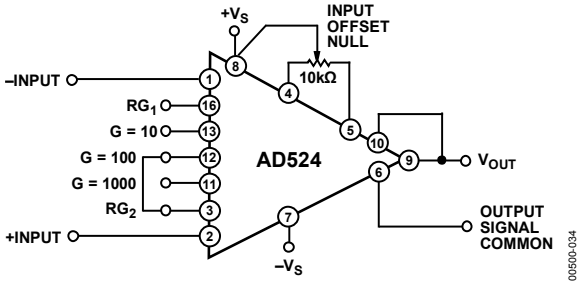

Figure 34. Operating Connections for G = 100

The AD524 can be configured for gains other than those that are internally preset; there are two methods to do this. The first method uses just an external resistor connected between Pin 3 and Pin 16 (see Figure 35), which programs the gain according to the following formula:

$$R_G = \frac{40\ \text{k}\Omega}{G-1}$$

NOTE: Typo here. The denominator should be G-1.

For best results, R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−50 ppm/°C typical).

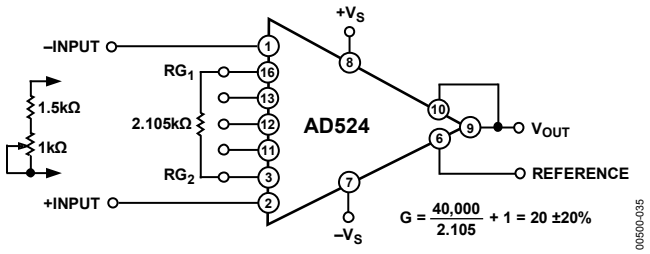

Figure 35. Operating Connections for G = 20

The second method uses the internal resistors in parallel with an external resistor (see Figure 36). This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

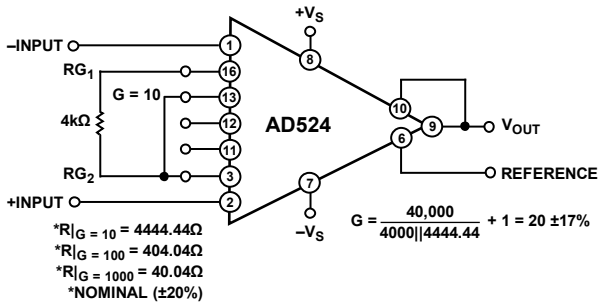

Figure 36. Operating Connections for G = 20, Low Gain Temperature Coefficient Technique

The AD524 can also be configured to provide gain in the output stage. Figure 37 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2, and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 precisely sets the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

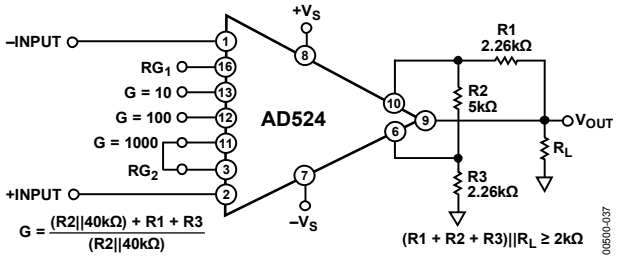

Figure 37. Gain of 2000

Table 4. Output Gain Resistor Values

Output Gain	R2	R1, R3	Nominal Gain
2	5 kΩ	2.26 kΩ	2.02
5	1.05 kΩ	2.05 kΩ	5.01
10	1 kΩ	4.42 kΩ	10.1

INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in a total error budget. The bias currents, when multiplied by the source resistance, appear as an offset voltage. What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature. Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source impedance imbalance.

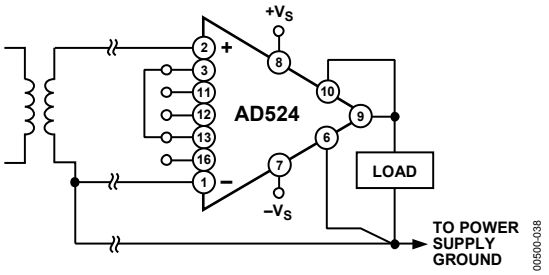

Figure 38. Indirect Ground Returns for Bias Currents—Transformer Coupled

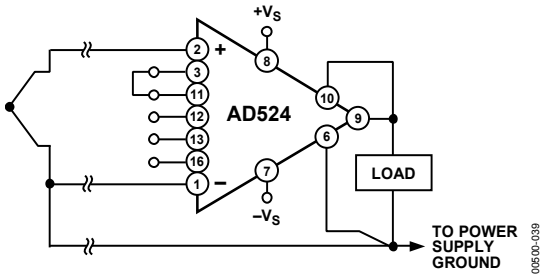

Figure 39. Indirect Ground Returns for Bias Currents—Thermocouple

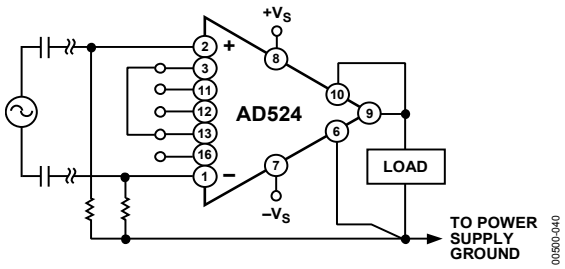

Figure 40. Indirect Ground Returns for Bias Currents–AC-Coupled

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying floating input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. Common-mode rejection ratio (CMRR) is a ratio expression whereas common-mode rejection (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80 dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications, shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figure 41 and Figure 42 show active data guards that are configured to improve ac common-mode rejection by bootstrapping the capacitances of the input cabling, thus minimizing differential phase shift.

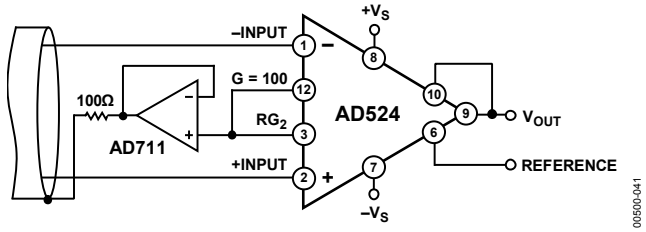

Figure 41. Shield Driver, G ≥ 100

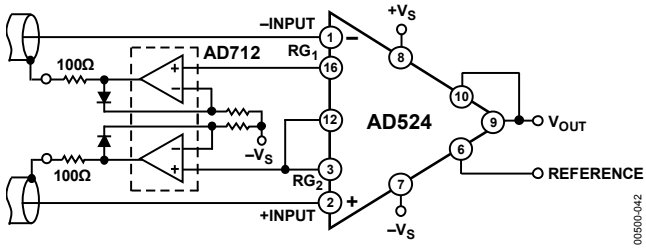

Figure 42. Differential Shield Driver

GROUNDING

Many data acquisition components have two or more ground pins that are not connected together within the device. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, because current flows through the ground wires and etch stripes of the circuit cards, and because these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to minimize the current flow in the path from the sensitive points to the system ground point. In this way, supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Because the output voltage is developed with respect to the potential on the reference terminal, an instrumentation amplifier can solve many grounding problems.

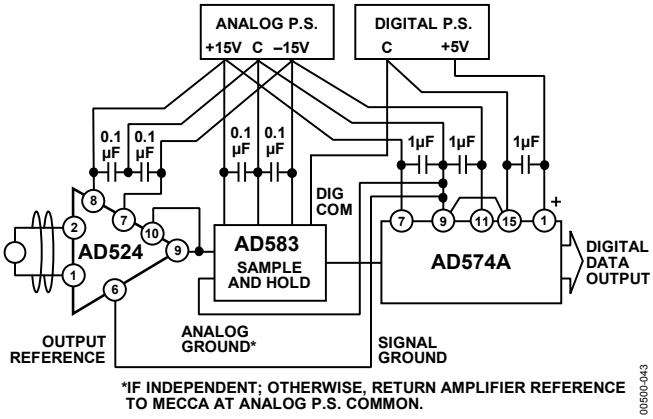

Figure 43. Basic Grounding Practice

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally, it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load, thus putting the IxR drops inside the loop and virtually eliminating this error source.

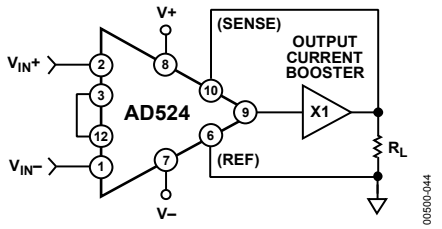

Figure 44. AD524 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2 kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 44 shows how a high current booster may be connected inside the loop of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities and offset and gain inaccuracies of the buffer are minimized by the loop gain of the AD524 output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal can be used to offset the output by up to ±10 V. This is useful when the load is floating or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 V to be shared between signal and reference offset.

When the AD524 is of the 3-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal.

Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path, thereby upsetting the common-mode rejection of the AD524.

In the AD524, a reference source resistance unbalances the CMR trim by the ratio of 20 kΩ/R_{REF}. For example, if the reference source impedance is 1 Ω, CMR is reduced to 86 dB (20 kΩ/1 Ω = 86 dB). An operational amplifier can be used to provide that low impedance reference point, as shown in Figure 45. The input offset voltage characteristics of that amplifier adds directly to the output offset voltage performance of the instrumentation amplifier.

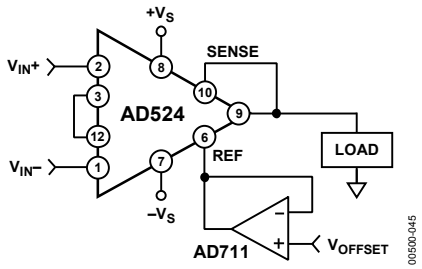

Figure 45. Use of Reference Terminal to Provide Output Offset

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals, as shown in Figure 46.

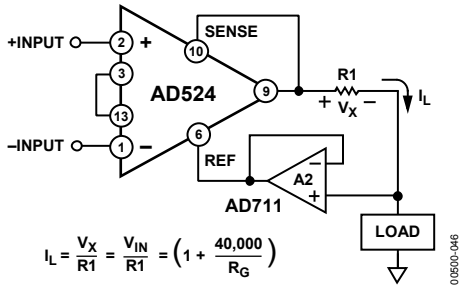

Figure 46. Voltage-to-Current Converter

By establishing a reference at the low side of a current setting resistor, an output current may be defined as a function of input voltage, gain, and the value of that resistor. Because only a small current is demanded at the input of the buffer amplifier (A2) the forced current, I_L, largely flows through the load. Offset and drift specifications of A2 must be added to the output offset and drift specifications of the AD524.

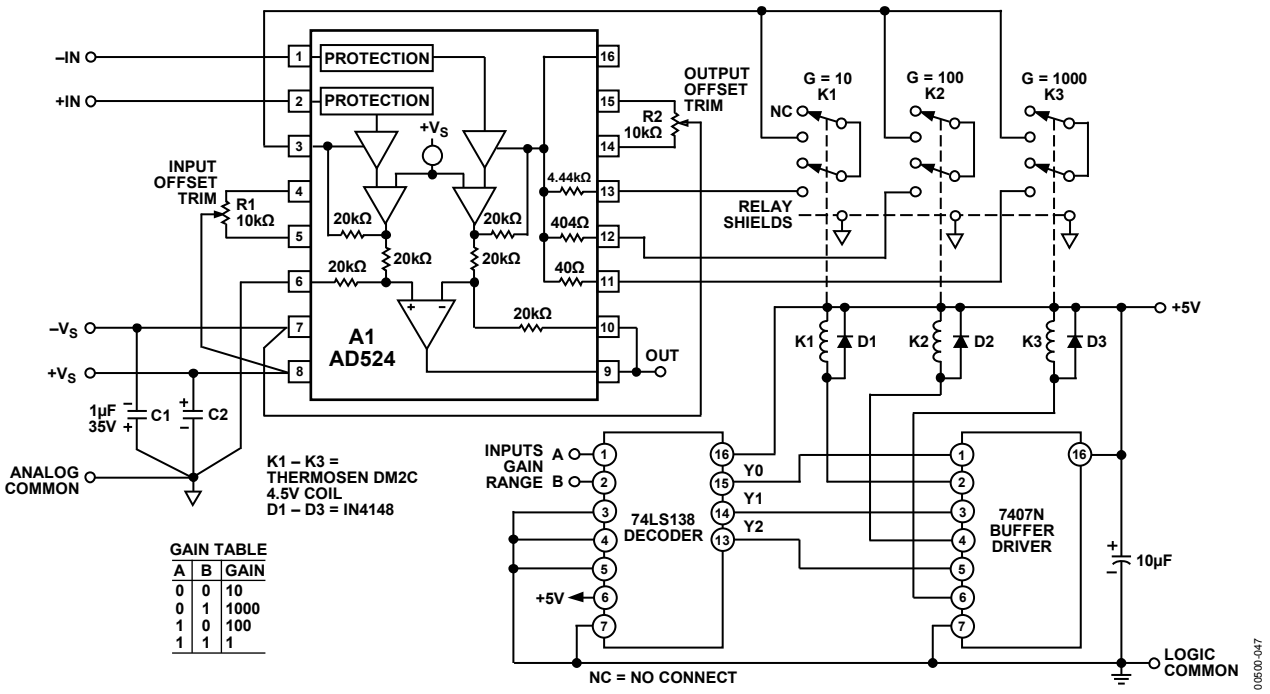

Figure 47. Three-Decade Gain Programmable Amplifier