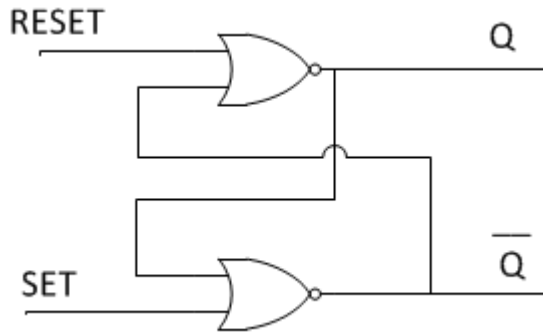


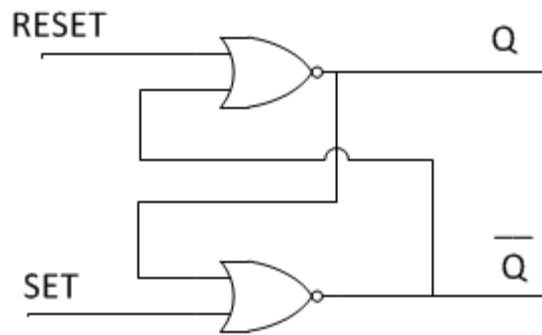
EET-210 Lab

R S NOR Latch (Active HIGH) Worksheet

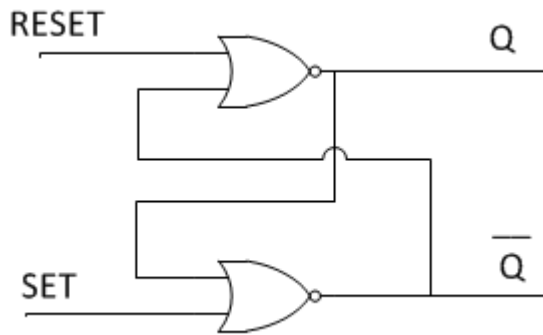
Q=0 initially ***Q=1 initially***



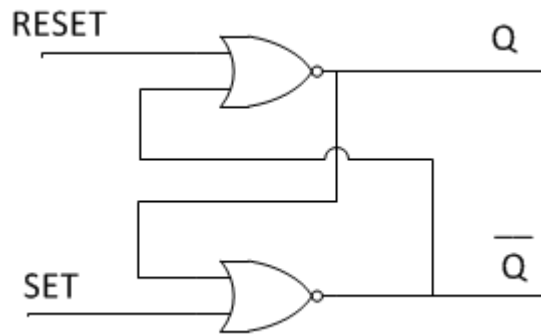
Circuit #1



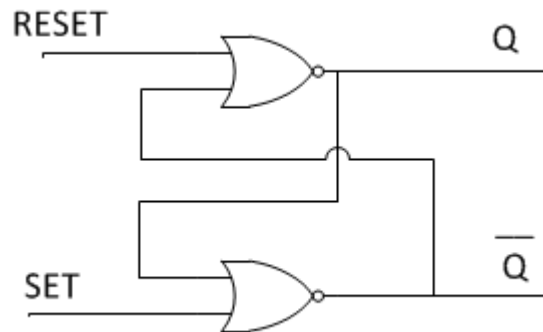
Circuit #2



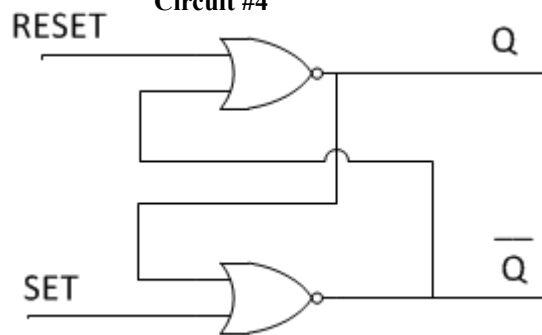
Circuit #3



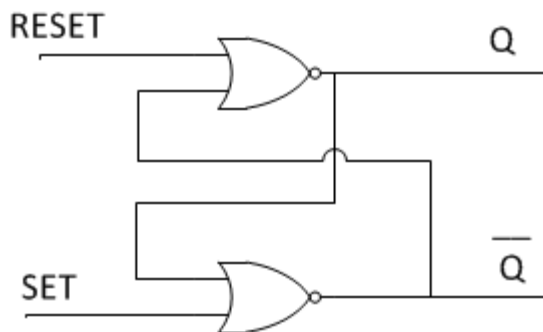
Circuit #4



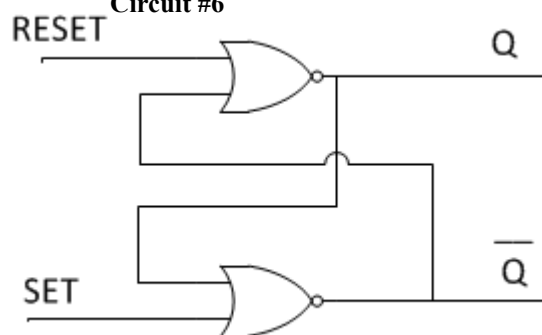
Circuit #5



Circuit #6



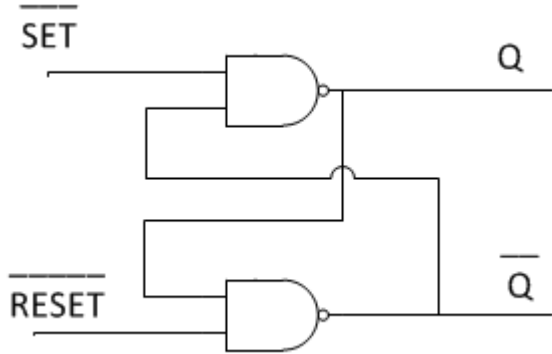
Circuit #7



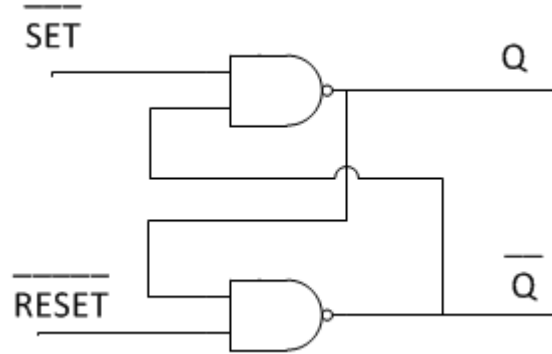
Circuit #8

$\overline{R} \overline{S}$ NAND Latch (Active LOW) Worksheet

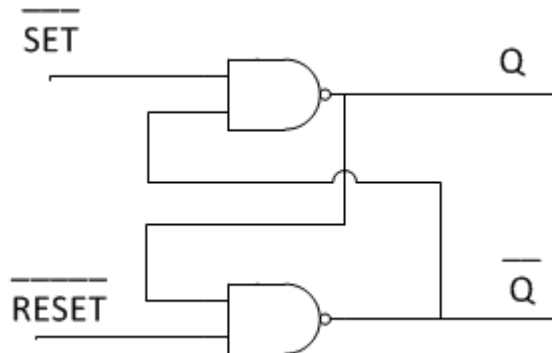
$Q=0$ initially $Q=1$ initially



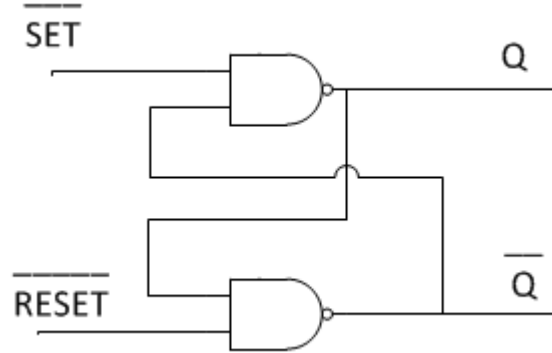
Circuit #1



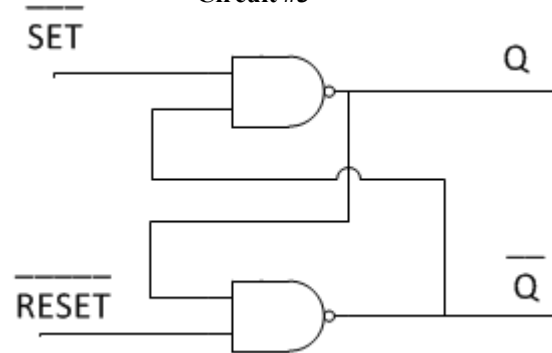
Circuit #2



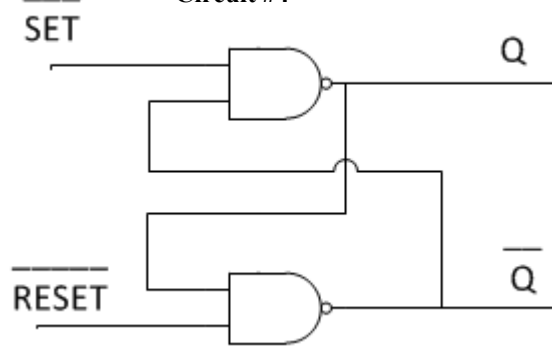
Circuit #3



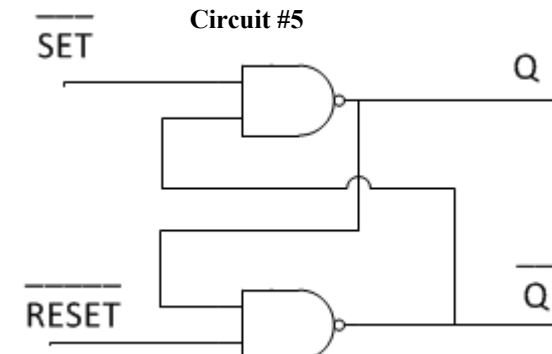
Circuit #4



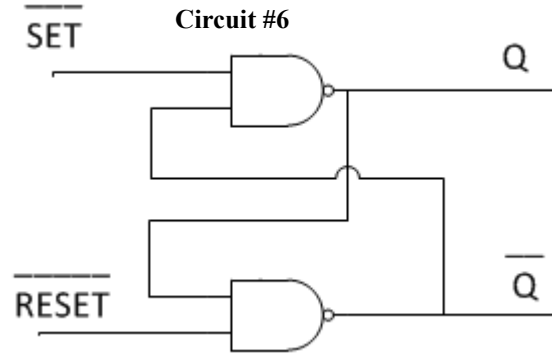
Circuit #5



Circuit #6



Circuit #7



Circuit #8

Truth Tables for NOR and NAND Latches

Notes:

S = SET: The SET state is defined when Q goes HIGH.

R = RESET: The RESET state is defined when Q goes LOW.

The SET and RESET states will occur with the input **S** and **R** inputs are HIGH, respectively. That is, they are active HIGH signals for the NOR latch.

Q and \bar{Q} should never be equal as this contradicts the definition of complement.

Q_n = initial state of Q.

Q(n+1) = the next stable state of Q.

R	S	Q _n	Q(n+1)	$\bar{Q}(n+1)$	State Name	Comments
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

RS NOR Latch – Complete Truth Table

R	S	Q(n+1)	$\bar{Q}(n+1)$	State Name
0	0			
0	1			
1	0			
1	1			

RS NOR Latch – Simplified Truth Table

$\overline{R} \overline{S}$ NAND Latch

Notes:

The SET and RESET states will occur with the input \overline{S} and \overline{R} inputs are LOW, respectively. That is, they are active LOW signals for the NAND latch..

$\overline{S} = \overline{SET}$: The SET state is defined when Q goes HIGH and will occur when \overline{S} is LOW.

$\overline{R} = \overline{RESET}$: The RESET state is defined when Q goes LOW and will occur when \overline{R} is LOW.

\overline{R}	\overline{S}	Q_n	$Q(n+1)$	$\overline{Q}(n+1)$	State Name	Comments
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

$\overline{R} \overline{S}$ NAND Latch – Complete Truth Table

\overline{R}	\overline{S}	$Q(n+1)$	$\overline{Q}(n+1)$	State Name
0	0			
0	1			
1	0			
1	1			

$\overline{R} \overline{S}$ NAND Latch – Simplified Truth Table