EET-210L TTL Logic Gate Operation with Pulse Signals

For this experiment, you will view the input/output relationship of a pulse signal applied to the standard types of logic gates. You will do this for each of the following gates: NOT (Inverter), AND, OR, NAND, NOR & XOR.

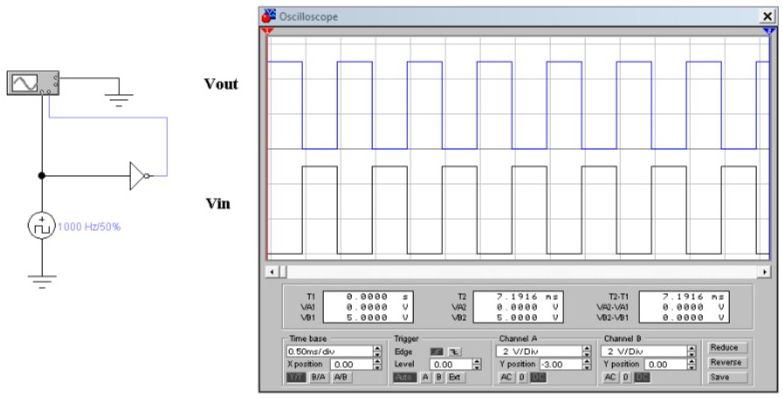
You will take two screenshots of each input & output signal for each type of gate (one screenshot for the NOT gate) for a total of 11 screenshots. Your screenshot should include your name or initials and the max, min & Frequency of the input signal and the Peak-Peak voltage of the output signal. You should post the screenshots for the NOT, AND & XOR gates (5 pics) with a description of the conditions for each screenshot. Keep the other screenshots for future reference.

You will only need to use one gate from each chip. For the inverter circuit, you will apply the TTL compatible* input voltage (0-5Vpp square wave & 1000 Hz) to the input, and observe the input and output signals simultaneously on the oscilloscope. For the other gates, one input will be connected to one of the logic switches on the PAD-234 Trainer.

***NOTE:** *The TTL compatible signal MUST be between 0V and 5V. In order to create this pulse, you have to add a 2.5 VDC offset voltage to the $5V_{p\text{-}p}$ square wave signal. If you don't do this, your input signal will be -2.5V to +2.5V. Also your scope inputs must be set to DC coupling to preserve the DC content present in TTL level signals.*

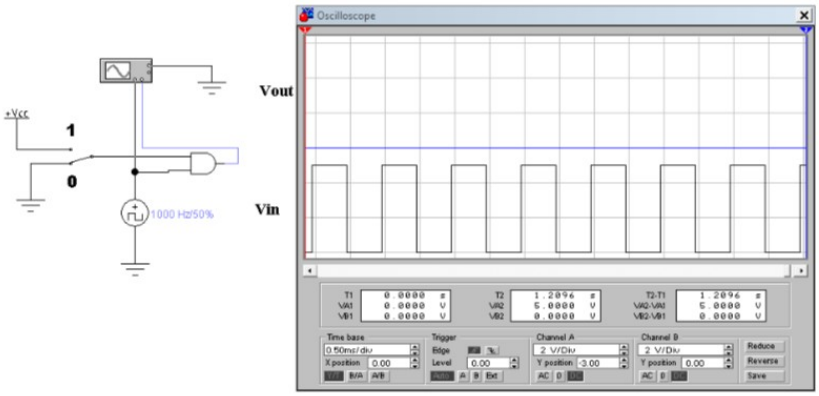
Sample Circuit Setups:

Inverter:

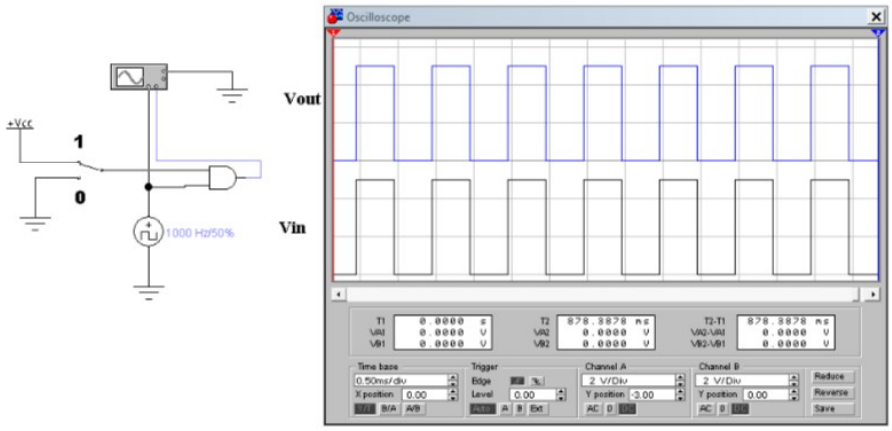


For the two input gates, you will take one screenshot with the switch in the 0 position and one screenshot with the switch in the 1 position.

AND Gate:
Switch = 0



AND Gate:
Switch = 1



Make similar screenshot using each of the other 2 input gates and post the screenshots specified earlier in the lab.