EET-210 Lab # Op-Amp Experiments #2 **Week #9.**

This week you will need the homework assignment *Op-Amp Lab and Practice Problems.pdf* posted in the Week #9 Forums for EET-210 Lecture. Based upon the op-amp Lab & Practice Problems sheets construct each of the circuits for the following problems.pdf

The data sheet for the 741 op-amp and a pdf of this assignment are also available in the Week #9 Forum.

Step #1: Fig. P3-4 is the circuit for problems 3-5 through 3-8. Calculate and verify by building each circuit and comparing your measured output to your expected (calculated) output. For Problem 8, increase your input signal to the maximum. If the op-amp does not go into saturation, reduce your power supply voltages until the op-amp saturates (you'll see a "clipped" output signal) on both the positive and negative output swings. For each problem, grab screenshots of Vin & Vout vs. time and Vin vs. Vout (XY Mode) with relevant measurements and your name on the display. Post these on the Week #9 Forum.

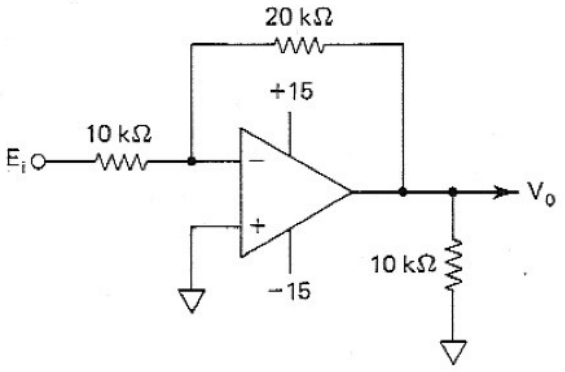

Figure P3-4

3-5. Calculate V_o and the op amp's output current in Fig. P3-4 if E_1 equals (**a**) +5 V; (**b**) −2 V. For each situation, state if the op amp sources or sinks current.

3-6. Calculate E_i in Fig. P3-4 if V_o equals (**a**) +5 V; (**b**) −2 V.

3-7. Let E_i be a triangle wave with a frequency of 100 Hz and a peak value of 5 V in Fig. P3-4. (**a**) Plot E_i and V_o vs. time; (**b**) V_o vs. E_i.

3-8. Repeat problem 3-7 but let E_i be increased in amplitude to 8 V. (Assume that $\pm V_{sat}$ = ±15 V for ease of plotting.)

Step #2: Build and verify a circuit which implements plot B. Is this an inverting or non-inverting amplifier? Take screenshots of Vin & Vout vs. time and Vin vs. Vout (XY Mode).

3-13. Input–output characteristics are shown for three different circuits in Fig. P3-13. Design circuits to recreate plots A, B, and C.

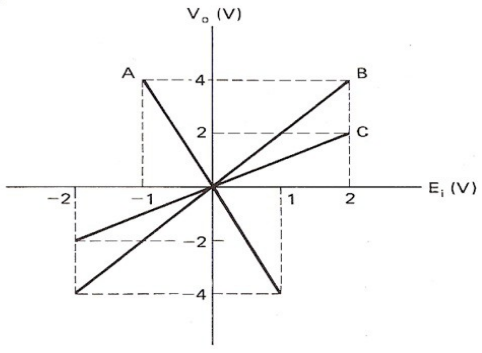

Figure P3-13

Step #3: Build and verify this circuit. It's recommended you use convenient D.C. sources for E_1 and E_2. (You'll need 2 741 IC's. Make all resistors the same value but they DO NOT have to be 10K, you can use any value between 2.2k - 47k as available.)

3-14. The circuit of Fig. P3-14 is called a "subtractor." Is E_i subtracted from E_2 or vice versa?

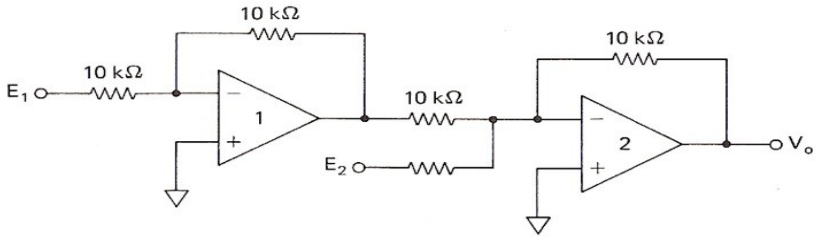

Figure P3-14

Step #4: Draw the schematic diagram, then build and verify the circuit in problem 3-17. Use the Superposition Principle (put a signal to each input individually while the other inputs are "off" (shorted)) and see if the summed output equals the output with all three source "on" simultaneously. For convenience, you can have all three sources be the same (e.g. 0.5V or 0.75V)

3-17. Design a three-channel inverting amplifier. Gains are to be -1 for channel 1, -3 for channel 2, and -5 for channel 3 (refer to Section 3-3.2).

Have your instructor initial this sheet as your receipt that you completed the assignment. Then post your relevant screenshots on the EET-210 Lab Forum for this assignment.

Instructor Initial_____